

ABSTRACT OF THE DISCLOSURE

Provided are exemplary methods for forming a semiconductor devices incorporating silicide layers formed at temperatures below about 700 °C., such as nickel silicides, that are formed after completion of a silicide blocking layer (SBL). The formation of the SBL tends to deactivate dopant species in the gate, lightly-doped drain and/or source/drain regions. The exemplary methods include a post-SBL activation anneal either in place of or in addition to the traditional post-implant activation anneal. The use of the post-SBL anneal produces CMOS transistors having properties that reflect reactivation of sufficient dopant to overcome the SBL process effects, while allowing the use of lower temperature silicides, including nickel silicides and, in particular, nickel silicides incorporating a minor portion of an alloying metal, such as tantalum, that exhibits reduced agglomeration and improved temperature stability.